IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A circuit comprising:

a first driver to receive a first signal from a first input port;

a second driver to receive a time-delayed version of the first signal from a second input port; and

a transformer coupled to the first driver and the second driver, the transformer to provide an output signal to an output port , the output signal being a half-raised cosine signal corresponding to the first signal and the second signal.

2. (Original) The circuit of claim 1, further comprising a capacitive load coupled to the transformer.

3. (Currently Amended) ~~The circuit of claim 2,~~ A circuit comprising:

a first driver to receive a first signal from a first input port;

a second driver to receive a time-delayed version of the first signal from a second input port;

a transformer coupled to the first driver and the second driver, the transformer to provide an output signal to an output port; where ~~wherein~~ the transformer has a leakage inductance and the capacitive load has a capacitance, and the time-delayed version of the first signal is time-delayed with respect to the first signal by a time about equal to a product of pi and a square-root of a product of the leakage inductance and the capacitance ; and

a capacitive load coupled to the transformer.

4. (Currently Amended) The circuit of claim 3 [[1]], further comprising an inductor coupled to the transformer and a transistor coupled to the inductor.

5. (Currently Amended) ~~The circuit of claim 4,~~ A circuit comprising:

a first driver to receive a first signal from a first input port;

a second driver to receive a time-delayed version of the first signal from a second input port;

a transformer coupled to the first driver and the second driver, the transformer to provide an output signal to an output port;

an inductor coupled to the transformer and a transistor coupled to the inductor in which ~~wherein~~ the inductor has an inductance and the transistor has a capacitance and the time-delayed version of the first signal is time-delayed with respect to the first signal by a time about equal to a product of pi and a square-root of a product of the inductance and the capacitance ; and

an inductor coupled to the transformer and a transistor coupled to the inductor .

6. (Currently Amended) The circuit of claim 5 [[1]], further comprising a Schmitt trigger circuit to couple the output port to the second input port.

7. (Original) The circuit of claim 6, wherein the Schmitt trigger circuit includes a hysteresis value about equal to a supply potential.

8. (Original) The circuit of claim 7, further comprising a clamp circuit coupled to the output port, the clamp circuit to hold the output port at the supply potential.

9. (Currently Amended) An apparatus comprising:

a plurality of circuits, each of the plurality of circuits including a plurality of drivers coupled to a first transformer circuit, wherein the first transformer circuit in each of the plurality of circuits is coupled to a second transformer circuit including a center-tap and each of the plurality of drivers in each of the plurality of driver circuits is coupled to a separate input port ; and

an output port connected to the center tap producing a half-raised cosine output signal corresponding to signals on each of the separate input port.

10. (Original) The apparatus of claim 9, wherein the first transformer circuit in at least one of the plurality of driver circuits comprises a loosely coupled transformer.

11. (Original) The apparatus of claim 10, further comprising a capacitive load coupled to the center-tap.

12. (Currently Amended) ~~The apparatus of claim 11,~~ An apparatus comprising:
a plurality of circuits, each of the plurality of circuits including a plurality of drivers coupled to a first transformer circuit, [wherein] the first transformer circuit in each of the plurality of circuits is coupled to a second transformer circuit including a center-tap and each of the plurality of drivers in each of the plurality of driver circuits is coupled to a separate input port, where the first transformer circuit in at least one of the plurality of driver circuits comprises a loosely coupled transformer, and

a capacitive load coupled to the center- tap, and [wherein] the capacitive load comprises a complementary metal-oxide field-effect transistor.

13. (Currently Amended) The apparatus of claim 12 [[9]], wherein the second transformer comprises an auto-transformer.

14. (Currently Amended) An apparatus comprising:

a communication circuit formed on a substrate; and

a power supply circuit formed on the [[die]] substrate to provide power to the communication circuit, the power supply circuit including:

a first driver coupled to an input port;

a delay circuit coupled to the input port;

a second driver coupled to the delay circuit; and

an auto-transformer coupled to the first driver, to the second driver, and to an output port, the output port being coupled to a capacitive load and the capacitive load being coupled to the communication circuit to provide power to the communication circuit.

15. (Original) The apparatus of claim 14, wherein the communication circuit comprises a communication base station.

16. (Original) The apparatus of claim 15, wherein the transformer includes a leakage inductance, the capacitive load includes a capacitance, and the delay circuit includes a delay about equal to a product of pi and the square-root of a product of the leakage inductance and the capacitance.

17. (Original) The apparatus of claim 16, wherein the processor comprises a reduced instruction set processor.

18. (Original) The apparatus of claim 14, further comprising a processor coupled to the communication circuit.

19. (Original) The apparatus of claim 18, wherein the processor comprises a very-long instruction word processor.

20. (Original) A method comprising:

receiving a first input signal;

receiving a second input signal, the second input signal being a time-delayed version of the first input signal; and

processing the first input signal and the second input signal to generate a half-raised cosine signal.

21. (Original) The method of claim 20, wherein receiving the first input signal comprises receiving a digital signal.

22. (Original) The method of claim 21, wherein receiving the second input signal comprises receiving a digital signal.

23. (Original) The method of claim 22, wherein processing the first input signal and the second input signal comprises providing a signal path including a first driver, an inductor, and a capacitive load for the first input signal and a signal path including a second driver, the inductor, and the capacitive load for the second input signal.

24. (Original) The method of claim 20, wherein receiving the first input signal comprises receiving a low-to-high transition signal.